IN THE CLAIMS:

Please cancel claims 9-20 without prejudice or disclaimer

1. (original) A multi-threading processor, comprising:

a first instruction fetch unit and a second instruction fetch unit;

a multi-thread scheduler unit coupled to said first instruction fetch unit and said second instruction fetch unit;

an execution unit coupled to said scheduler unit, wherein said execution unit is to execute a first active thread and a second active thread; and

a register file coupled to said execution unit, wherein said register file is to switch one of said first active thread and said second active thread with a first inactive thread.

2. (previously presented) A multi-threading processor as recited in claim 1, further comprising an on deck context unit coupled to the register file, wherein said on deck context unit is to maintain the first inactive thread and a second inactive thread.

3. (previously presented) A multi-threading processor as recited in claim 2, wherein said register file is to switch one of the first active thread and the second active thread with the second inactive thread.

4. (original) A multi-threading processor as recited in claim 3, further comprising:

a first instruction decode unit coupled between the first instruction fetch unit and the scheduler unit; and

a second instruction decode unit coupled between the second instruction fetch unit and the scheduler unit.

5. (original) A multi-threading processor as recited in claim 1, wherein the scheduler unit is a four thread scheduler unit, further comprising:

a third instruction fetch unit coupled to said four thread scheduler unit; and

a fourth instruction fetch unit coupled to said four thread scheduler unit.

6. (original) A multi-threading processor as recited in claim 5, wherein said register file is a four way register file.

7. (original) A multi-threading processor as recited in claim 6, wherein said register file is to switch one of the first active thread and the second active thread with a second inactive thread.

8. (original) A multi-threading processor as recited in claim 7, further comprising:

a third instruction decode unit coupled between the third instruction fetch unit and the four thread scheduler unit; and

a fourth instruction decode unit coupled between the fourth instruction fetch unit and the four thread scheduler unit.

9-20. (canceled).